AMENDMENTS TO THE CLAIMS

Please cancel Claim 3 without prejudice, as indicated below.

Please amend Claims 1, 8, 17, and 20, as indicated below.

A complete listing of all claims is presented below with insertions underlined (e.g., insertion), and deletions struckthrough or in double brackets (e.g., ~~deletion~~ or [[deletion]]):

1. (Currently Amended) A memory module comprising:

a printed circuit board having an edge, a first side, and a common signal trace connector area positioned along the edge, the printed circuit board having a plurality of interconnection levels;

a first row of integrated circuits identical to one another, the first row mounted on the first side of the printed circuit board, the first row being substantially parallel to the edge and in proximity to the common signal trace connector area, the integrated circuits of the first row having a first orientation direction;

a second row of integrated circuits identical to the integrated circuits of the first row, the second row mounted on the first side of the printed circuit board, the second row being substantially parallel to the edge and in proximity to the first row and located physically farther from the common signal trace connector than is the first row, the integrated circuits of the second row having a second orientation direction different from the first orientation direction;

a first plurality of data lines electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area, each data line of the first plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length; and

a second plurality of data lines electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area, each data line of the second plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length, each data line having a length substantially equal to a sum of the trace portion lengths of the data line, whereby lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same.

2. (Original) The memory module of Claim 1, wherein the second orientation direction is rotated in a plane parallel to the printed circuit board by approximately 180 degrees from the first orientation direction.

3. (Cancelled)

4. (Original) The memory module of Claim 1, wherein the printed circuit board has a line of bilateral symmetry which is substantially perpendicular to the edge and which bisects the printed circuit board into a first lateral half and a second lateral half.

5. (Original) The memory module of Claim 4, wherein the first row is bilaterally symmetric with respect to the line of bilateral symmetry.

6. (Original) The memory module of Claim 4, wherein the second row is bilaterally symmetric with respect to the line of bilateral symmetry.

7. (Original) The memory module of Claim 4, wherein a first set of address signal paths connect the integrated circuits of the first row and the second row on the first lateral half to a first common register and a second set of address signal paths connect the integrated circuits of the first row and the second row on the second lateral half to a second common register, the first set of address signal paths and the second set of address signal paths being bilaterally symmetric to one another across the line of bilateral symmetry.

8. (Currently Amended) A method for arranging integrated circuit locations on a printed circuit board for a memory module, the method comprising:

providing a printed circuit board having an edge, a first side, and a common signal trace connector area positioned along the edge, the printed circuit board having a plurality of interconnection levels;

mounting a first row of integrated circuits identical to one another on the first side of the printed circuit board, the first row being substantially parallel to the edge and in proximity to the common signal trace connector area, the integrated circuits of the first row having a first orientation direction;

mounting a second row of integrated circuits on the first side of the printed circuit board, the integrated circuits of the second row identical to the integrated circuits of the first row, the second row being substantially parallel to the edge and in proximity to the first row and located physically farther from the common signal trace connector than is

the first row, the integrated circuits of the second row having a second orientation direction different from the first orientation direction;

electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area by a first plurality of data lines, each data line of the first plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length; and

electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area by a second plurality of data lines, each data line of the second plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length, each data line having a length substantially equal to a sum of the trace portion lengths of the data line, whereby lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same.

9. (Original) The method of Claim 8, wherein the second orientation direction is rotated in a plane parallel to the printed circuit board by approximately 180 degrees from the first orientation direction.

10. (Original) The method of Claim 8, wherein the printed circuit board has a line of bilateral symmetry which is perpendicular to the edge and which bisects the printed circuit board into a first lateral half and a second lateral half.

11. (Original) The method of Claim 10, wherein the first row is bilaterally symmetric with respect to the line of bilateral symmetry.

12. (Original) The method of Claim 10, wherein the second row is bilaterally symmetric with respect to the line of bilateral symmetry.

13. (Original) The method of Claim 10, further comprising:

interconnecting the integrated circuits of the first row and the second row on the first lateral half to a first common register by a first set of address signal paths; and

interconnecting the integrated circuits of the first row and the second row on the second lateral half to a second common register by a second set of address signal paths, wherein the first set of address signal paths and the second set of address signal paths are bilaterally symmetric to one another across the line of bilateral symmetry.

14. (Original) The method of Claim 8, further comprising:

interconnecting the integrated circuits in a first portion of the first row and the integrated circuits in a first portion of the second row to a first register location; and

interconnecting the integrated circuit locations in a second portion of the first row and the integrated circuit locations in a second portion of the second row to a second register location.

15. (Original) The method of Claim 14, wherein the first portion of the first row comprises a first half of the first row, and the first portion of the second row comprises first half of the second row.

16. (Original) The method of Claim 14, wherein the second portion of the first row comprises a second half of the first row, and the second portion of the second row comprises a second half of the second row.

17. (Currently Amended) A memory module comprising:

a printed circuit board having an edge, a first side, and a common signal trace connector area positioned along the edge, the printed circuit board having a plurality of interconnection levels;

a first row of integrated circuits identical to one another, the first row mounted on the first side of the printed circuit board, the first row being substantially parallel to the edge and in proximity to the common signal trace connector area, the integrated circuits of the first row having a first orientation direction;

a second row of integrated circuits identical to the integrated circuits of the first row, the second row mounted on the first side of the printed circuit board, the second row being substantially parallel to the edge and in proximity to the first row and located physically farther from the common signal trace connector than is the first row, the integrated circuits of the second row having a second orientation direction different from the first orientation direction; and

means for electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area via different interconnection levels of the printed circuit board and for electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area via different interconnection levels of

the printed circuit board, whereby corresponding trace lengths to the first row of integrated circuits and the second row of integrated circuits are substantially the same.

18. (Original) The memory module of Claim 17, wherein the second orientation direction is rotated in a plane parallel to the printed circuit board by approximately 180 degrees from the first orientation direction.

19. (Original) The memory module of Claim 17, wherein the printed circuit board has a line of bilateral symmetry which is perpendicular to the edge and which bisects the printed circuit board into a first lateral half and a second lateral half.

20. (Currently Amended) The memory module of Claim [[17]]19, further comprising bilaterally symmetric means for interconnecting the integrated circuits of the first row and the second row on the first lateral half to a first common register and for interconnecting the integrated circuits of the first row and the second row on the second lateral half to a second common register.